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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,476	12/27/2001	Jae Yong Park	8733.571.00	7764
30827	7590	05/04/2004	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP			ALEMU, EPHREM	
1900 K STREET, NW			ART UNIT	
WASHINGTON, DC 20006			PAPER NUMBER	
			2821	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/026,476

Applicant(s)

PARK ET AL.

Examiner

Ephrem Alemu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2004.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
4a) Of the above claim(s) 7-12 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-6 and 12-14 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (US 6,462,722).

Re claims 1, 2, 12 and 13, Kimura discloses an active matrix organic electroluminescence display (Fig. 1) device comprising:

- a scan line (111) in one direction (Fig. 1; Col. 3; lines 13-17);
- a data line (112) substantially perpendicular to the scan line (111) (Fig. 1; Col. 3; lines 13-17);
- a power line (i.e., common line 114) substantially parallel to the data line (112) keeping a distance with the data line (112) (Fig. 1);
- an electroluminescence device (131) emitting light in a pixel region among the scan line (111), the data line (112) and the power line (i.e., common line 114) (Fig. 1; Col. 3; lines 13-35);
- a switching transistor (121) for switching a signal of the data line (112) according to a signal of the scan line (111) (Fig. 1; Col. 3; lines 19-34); and
- a driving transistor (122) for applying a power supply of the power line (i.e., common line 114) to the electroluminescence device (131) according to a signal applied through the switching transistor (121) (Fig. 1; Col. 3; lines 29-53).

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Although, Kimura discloses the channel region of the switching transistor (121) or the driving transistor (122) being made of polycrystalline silicon (Col. 10, lines 12-22); Kimura does not teach the polycrystalline silicon of the channel region of the switching transistor (121) or the driving transistor (122) having a longitudinal grain and the longitudinal grain being substantially parallel to a current flow direction of the channel region.

However, it is widely known in the art that the current flows along the channel region of a transistor and since transistor are fabricated to optimize the current flow along the channel region.

Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to align the grain of the polycrystalline silicon substantially parallel to the current flow direction in the channel region for optimizing the current flow in the channel region of the transistors.

Re claims 2 and 3, the limitation that the longitudinal grain being formed by a sequential lateral solidification (SLS) method is not given patentable weight because, this is considered a product-by-process claim. "Even though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), *Ex parte Edwards* 231 USPQ 981, 983 (BdPatApp&Int 1986).

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Re claims 3 and 14, Kimura further discloses a capacitor (123) storing electrons according to a difference between a voltage of data signal applied to the data line (112) and a voltage provided from the power line (i.e., common line 114) (Fig. 1).

Re claims 4 and 6, Kimura discloses an active matrix organic electroluminescence display device (Fig. 4) comprising:

- a plurality of scan lines (111) in one direction (Fig. 1; Col. 3; lines 13-17);

- a plurality of data lines (112) substantially perpendicular to the scan lines (111) to define a plurality of pixel regions (7) (Fig. 1; Col. 3; lines 13-17);

- a plurality of power lines (i.e., common line 114) substantially parallel to the data line (112) keeping a distance with the data line (112) (Fig. 1);

- an electroluminescence device (131) emitting light in each of the pixel regions (7) among the scan line (111), the data line (112) and the power line (i.e., common line 114) (Fig. 1; Col. 3; lines 13-35);

- a switching transistor (121) for switching a signal of the data line (112) according to a signal of the scan line (111) in each of the pixel regions (7) (Fig. 1; Col. 3; lines 19-34);

- a driving transistor (122) for applying a power supply of the power line (i.e., common line 114) to the electroluminescence device (131) according to a signal applied through the switching transistor (121) in each of the pixel regions (7) (Fig. 1; Col. 3; lines 29-53);

- a gate driver IC (i.e., scanning-side drive circuit 4) having a plurality of transistors for applying a scan signal to each scan line (111); and a data driver IC (i.e., data-side

drive circuit 3) having a plurality of transistors for applying a data signal to each data line (112) (Fig. 1; Col. 3, lines 1-12).

Although, Kimura discloses the channel region of the transistors being made of polycrystalline silicon (Col. 10, lines 12-22); Kimura does not teach the polycrystalline silicon of the channel region of the transistors having a longitudinal grain and the longitudinal grain being substantially parallel to a current flow direction of the channel region.

However, it is widely known in the art that the current flows along the channel region of a transistor and since transistor are fabricated to optimize the current flow along the channel region.

Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to align the grain of the polycrystalline silicon substantially parallel to the current flow direction in the channel region for optimizing the current flow in the channel region of the transistors.

Re claims 5 and 6, the limitation that the switching transistor (121) and the driving transistor (122) can be formed by low temperature polysilicon low temperature process and a scanning method; and the longitudinal grain being formed by a sequential lateral solidification (SLS) method is not given patentable weight because, this is considered a product-by-process claim. "Even though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was

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made by a different process.” *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), *Ex parte Edwards* 231 USPQ 981, 983 (BdPatApp&Int 1986).

Response to Arguments

3. Applicant's arguments with respect to claim 1-6 and 12-14 have been considered but are moot in view of the new grounds of rejection.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Grigoropoulos et al. (US 6,451,631); also teaches similar inventive subject matter.

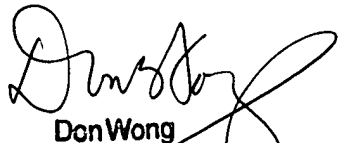
Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ephrem Alemu whose telephone number is (571) 272-1818. The examiner can normally be reached on M-F Flex hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don K Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA
4-28-04


Don Wong
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